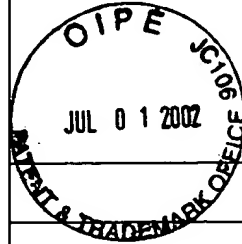


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List of Patents and Publications
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Disclosure Statement
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ATTY. DOCKET NO: 5150-23006

SERIAL NO: 09/788,219



APPLICANT: Kodosky et al.

FILING DATE: February 16, 2001

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U.S. PATENT DOCUMENTS

EXAM. INITIALS	REF. DES	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE
RF	A1	6,230,307	05/082001	Davis et al.	716	16	RECEIVED
RF	A2	6,226,776	05/01/2001	Panchul et al.	716	3	JUL 08 2002
RF	A3	5,603,043	02/11/1997	Taylor et al.	712	Technology Center 2100	
RF	A4	5,555,201	09/10/1996	Dangelo et al.	716	1	
RF		6,219,628	04-17-/2001	Kodosky et al.	703	2	
RF		5,684,980	11-04-1997	Casselman	703	23	
RF		5,535,342	07-09-1996	Taylor	710	315	
RF		5,652,875	07-29-1997	Taylor	716	1	
		5,603,043	02-11-1997	Taylor et al.			
RF		5,497,498	03-05-1996	Taylor	710	104	
RF		5,583,749	12-10-1996	Tredennick et al.	361	790	
RF		5,541,849	06-30-1996	Rostoker et al.	716	18	
RF		5,737,235	04-1998	Kean et al.	716	16	
RF		5,638,299	06-1997	Miller	702	127	
RF		5,309,556	05-1994	Sismilich	345	771	
RF		6,064,409	05-2000	Thomsen et al.	345	700	
RF		5,732,277	03-1998	Kodosky et al.	717	125	

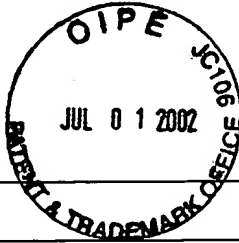
FOREIGN PATENT DOCUMENTS

EXAM. INITIALS	REF. DES	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB CLASS	TRANSLATION. YES/NO
RF		WO 94 10627 A	5/11/94	PCT	—	—	
RF		WO 94 15311 A	7/7/94	PCT	—	—	

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RF	XP0002087124 Xiao-Yu, et al., "Software Environment for WASMII: A Data Driven Machine with a Virtual Hardware," Field Programmable Logic Architectures, Synthesis and Applications, 4 th International Workshop on Field-Programmable Logic and Applications, FPL '94 Proceedings, Berlin, Germany, 1994.
RF	XP000554820 Edwards, et al., "Software acceleration using programmable hardware devices," IEEE Proceedings: Computers and Digital Techniques, vol. 143, no. 1, January 1996, pp. 55-63.
RF	XP000380758 Lesser, et al., "High Level Synthesis and Generating FPGAs with the BEDROC System," Journal of VLSI Signal Processing, vol. 6, no. 2, August 1993, pp. 191-214.
RF	International Search Report for PCT/US 98/13040 mailed 12/22/98.
RF	Ade, M; Lauwereins, R; Peperstraete, J.A.; Hardware-Software Codesign with GRAPE, Proceedings of the Sixth IEEE International Workshop on Rapid System Prototyping, pp. 40-47, 6/9/95.
RF	Lauwereins, R; Engels, M; Ade, M; Peperstraete, J; Grape-II: A System-Level Prototyping Environment for DSP Applications, Computer, Vol. 28, Issue 2, pp. 35-43, 2/95.
RF	Lysaght, P; Stockwood, J; A Simulation Tool for Dynamically Reconfigurable Field Programmable Gate Arrays, IEEE Transactions on Very Large Scale Integration Systems, Vol. 4, Issue 3, pp. 381-390, 9/96.
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RF	Boulay et al., A High Throughput Controller for a 256-Channel Cardiac Potential Overlapping System, Canadian Conference on Electrical and Computer Engineering, Vol. 1, pp. 539-542, September 1995.
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EXAMINER:

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DATE CONSIDERED:

21-MAR-03

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the patent owner.

Information Disclosure Statement--PTO 1449 (modified)

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